CONTROLLED LEAKAGE CMOS DECOUPLING CAPACITOR FOR APPLICATION SPECIFIC INTEGRATED CIRCUIT LIBRARIES

Background of the Invention

Technical Field of the Invention

5   This invention relates to electronic circuit design. More specifically, it relates to placement of voltage and ground contacts in a decoupling capacitor for application specific integrated circuit (ASIC) libraries.

Background Art

10   Current CMOS technology integrated circuits (ICs) contain millions of logic gates switching at very high speeds. Decoupling capacitors are required across the power supply busses VDD and GND to reduce the switching noise which can affect the timing of the individual gates on the

15   chip. As CMOS technologies have progressed, higher circuit speeds are realized and increased wire resistance results from smaller metal cross sections in the power bussing. Adding larger areas of decoupling capacitors to an IC

requires large areas of polysilicon which increase the probability that a single processing defect could cause a short from VDD to Ground in the capacitor area. This would render the entire chip useless and reduce the wafer yield

5   thereby increasing the cost of the functional chips.

Heretofore a first solution has been to add a gating device in series to the decoupling capacitor for two reasons: first, to turn off the leakage path from VDD to Ground for testing purposes; and, second, to gate off the

10   defective device to save the chip should a defect cause a power supply short in the capacitor area.

There are a few drawbacks to the above solution that make implementation difficult, and the usefulness of this approach is bandwidth limited for high speed applications.

15   The gating device is usually an NFET (NFET are typically smaller than PFET for the same lgs current). This NFET is sized such that there is a low impedance from gate-to-source. The low impedance in series with the capacitor is required to reduce the RC which limits the bandwidth of the

20   network. This low impedance NFET must be very large physically which may take up as much area as the capacitor itself. The large NFET must also have a large gate area

which increases the gate capacitance, which in turn forces the chip designer to use a large driver to drive the gate. Another draw back is the fact that the decoupling capacitor has an input pin. Ideally a decoupling capacitor is a passive device without any wireable pins. When thousands of decoupling capacitors are required on a chip, thousands of gates must be wired and driven by circuit buffers from one or more primary input pins. The wiring and buffering is further complicated when it is desirable to isolate and degate the defective capacitor. A substantial amount of circuit area and wireability is lost when implementing such schemes.

A second solution has involved the addition of an integrated circuit resistor, resulting in a capacitor with a large RC. This solution also results in a relatively large area requirement for the resistor.

It is understood that coupled noise and leakage are driving down circuit yields. This is cause by highly resistive and closely spaced circuit wiring (coupled noise) and extremely thin gate oxides causing current leakage. A large RC means that the capacitor can not function as a decoupling capacitor, or has limited affect as a decoupling

capacitor. On the other hand, a low series resistance capacitor allows more leakage current. Consequently, there is a need in the art for a decoupling capacitor the limits leakage current by design without adding a resistor in series.

Such decoupling capacitors as gated capacitors, capacitors with series resistance of a chosen resistance, and a series of capacitors pfet/nfet decoupler with NFET drain tied to PFET gate and Pfet drain tied to NFET gate which have previously done well at high-frequency decoupling have not performed successfully in newer technologies due to their large series resistance

Referring to Figures 1 and 2, the first solution described above uses a gating transistor TN2 102 that can be turned on or off by switching the input GATE 104 high or low. When turned off, such as during test, gate 102 is open. The leakage current through the capacitor CAP1 106 from VDD 110 to GND 108 is limited by the size of gating transistor TN2 102 when TN2 is on. This approach requires a very large device TN2 102, a buffer TN1 112 and TP1 114 and an input pin 100 for gate 104, all added to the layout of capacitor CAP1 106.

Referring to Figure 3, the second solution described above uses an integrated circuit resistor R1 116 added in series to capacitor CAP1 106. Referring to Figure 4, this solution requires the area overhead of the integrated circuit resistor 116, which reduces the layout density of decoupling capacitor CAP1 106 considerably.

Summary of the Invention

A decoupling capacitor includes a fixed resistance in series with the capacitor, the resistance formed by contacts connecting a polysilicon layer to metal and a diffusion layer to metal; the contacts being of location and quantity sufficient for limiting defect current while allowing the capacitor to function at high frequency.

Other features and advantages of this invention will become apparent from the following detailed description of the presently preferred embodiment of the invention, taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a schematic representation of a decoupling capacitor with NFET gate.

Figure 2 is a schematic representation of a portion of the decoupling capacitor of Figure 1, showing on and off

5   states.

Figure 3 is a schematic representation of a decoupling capacitor with integrated resistor.

Figure 4 is a schematic representation of the structure of the decoupling capacitor of Figure 3.

10   Figure 5 is a schematic representation of the decoupling capacitor of the present invention.

Figure 6 is a layout representation of the structure of the decoupling capacitor of Figure 5.

Figure 7 is a layout representation of the structure of

15   the decoupling capacitor of the present invention.

Figure 8 is a schematic representation of a decoupling capacitor, simplified to support illustration of the RC

circuit of Figure 9.

Figure 9 is a schematic representation of the resultant capacitor of Figure 8 shown as a distributed RC circuit.

Figure 10 illustrates a defect site in the insulation
5   layer of an electronic package.

Figure 11 illustrates typical circuit ties for the electronic package of Figure 10.

Figure 12 illustrates the package of Figure 10 modified in accordance with the present invention to establish
10   surface resistance as the dominant factor between voltage and ground in the presence of a defect.

Figures 13 and 14 illustrate patterns of surface current between voltage and ground planes in a package with a defect.

15   Figure 15 illustrates the dimension K of the present invention for assuring that surface resistance is the dominant factor between voltage and ground in the presence of a defect.

Figure 16 is flow chart illustrating the steps of a method in accordance with the present invention for determining contact site placement and number of contacts in an electronic package.

5   Figure 17 is a high level system diagram illustrating a program storage device readable by a machine, tangibly embodying a program of instructions executable by a machine to perform method steps for determining contact site placement and number of contacts in an electronic package.

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Best Mode for Carrying Out the Invention

The present invention solves problems associated with prior art approaches by replacing the gating device with a controlled resistance between the capacitor and ground. The

15   resistance is small enough to allow the RC of the decoupling capacitor to be useful for high frequency and large enough to limit the current due to a short circuit caused by a defect.

In accordance with the invention, a decoupling

20   capacitor that has a fixed resistance in series with the

capacitor is formed by contacts connecting polysilicon to
metal and diffusion to metal. The location and quantity of
these contacts serve to limit the leakage or defect current
and at the same time allow the decoupling capacitor to
5   function at high frequency. The absence of an additional
integrated circuit resistor or MOS device to limit current
reduces the area of the device considerably. A control pin
for the gating function is no longer necessary, which allows
more freedom of placement without any of the wiring overhead
10   of the prior solutions.

Referring to Figures 5 and 6, a schematic
representation of the present invention is similar to that
of Figures 3 and 4, respectively, but does not require the
additional integrated circuit resistor R1 116 shown in
15   Figure 3. In a sense, the present invention may be viewed as
providing a way to remove resister R1.

Of course, there still is resistance in the path from
Vdd - Capacitor - Gnd, due in a measure to the number of
contacts. However, as will be described hereafter, the
20   contact resistance to voltage and to ground ($R_{CA\ VDD}$ + $R_{CA\ GND}$)
is not the limiting factor. Under these conditions, a
defect shorting the polysilicon gate to the substrate forces

the current to travel from the Vdd contact through a section

of the substrate, then up to the polysilicon through the

defect, and finally along the rest of the polysilicon gate

to the ground contact. The resistance of that path is used

5   to limit any defect leakage current, and does so without the

addition of a resistor element 116 to the package, or

layout. Removing that resistor 116 from the layout means

that a much denser capacitor layout may be achieved. Also,

the removal of resistor 116, which typically is quite large,

10   reduces the overall RC, resulting in a decoupling capacitor

(decap) with a higher bandwidth compared to prior art

designs. This is important with technology pushing towards

higher frequency circuits. The present invention achieves

decoupling using a capacitor that operates over a higher

15   bandwidth due to the smaller series resistance.

Referring to Figure 7, more detailed schematic

representation of the present invention is presented. Two

plates 148, 150 form a capacitor, with a first voltage

(ground) on top plate 148 (the polysilicon layer) and a

20   second voltage (Vdd) on bottom plate 150 (the diffusion

layer). With very thin oxide, current may leak through the

capacitor. The layout in Figure 7 is that of a decoupling

capacitor that limits leakage current by the number and

location of contacts 144, 146. Current flow from the VDD

straps 140 located at the top and bottom of the cell to the

ground straps 142 located in the middle of the cell is

limited by the number of contacts connecting diffusion to

5   VDD and polysilicon to GND. A statistical analysis of the

contact resistance may be used to determine the minimum and

maximum resistance per contact. The total resistance

required is composed of the series/parallel combination

contacts equivalent to the desired value. The desired

10   minimum resistance sets the maximum leakage current and the

desired maximum resistance sets the overall RC of the

decoupling capacitor which will limit the bandwidth or

response of the RC network. The resistance target is broken

down into a number of contacts that connect the polysilicon

15   to the GND bus and the diffusion to the VDD buss providing

many parallel paths for current to flow while limiting the

current to a maximum value and limiting the bandwidth to the

maximum value.

Alternatively, the contacts may be distributed evenly

20   along the polysilicon and the diffusion contacts placed on

the opposite end of the capacitor. However, the illustrated

layout utilizes the VDD straps that are part of a background

image (meaning the VDD straps are there no matter what the

circuit is) to keep wiring tracks free. This makes
placement of the capacitor easier since it is easy to wire
circuits on the left of the capacitor to the circuits on the
right should the need arise.

5   The placement of the GND contacts to VDD contacts is
spread as far apart as possible (distance K 152) to force
leakage current through polysilicon and diffusion which
further limit the current due to the polysilicon and
diffusion resistance. Together the total resistance in
10   series for leakage is (where CA means "contact" and RX means
"diffusion"):

(1) $R_{leak} = R_{CA\ VDD} + R_{RX\ avg} + R_{PC\ avg} + R_{CA\ GND}$

The contact resistance should play a very small role in
the equation above because the contact resistance can vary
15   widely. To say that the leakage resistance can be limited
by only placing one contact on the polysilicon layer and one
contact on the diffusion layer would be a poor design
choice. The contact resistance can vary such that the total
leakage resistance is much smaller than expected, or the
20   contact resistance can be so large that the design is no
longer an effective decoupling capacitor. If the contact

resistance is too large, the charge needed to stabilize the

GND and VDD fluctuations, for example due to circuit

switching, might not be able to move from the plate to the

power rails quickly.

5   The contacts and the resistance they contribute play a

very small role in leakage resistance. Consequently, where

contacts are placed determines control on leakage. The

contact resistance is relatively minor in comparison with

the total resistance along the described path. An optimal

10   design requires that enough contacts be provided to assure

good connection between the plates of the capacitor and the

Vdd/Gnd buses, and putting as many contacts as available

space permits (as will be described hereafter) all but takes

the contact resistance out of the equation.

15   The worst case scenario would be where something causes

the Vdd and Gnd plates to short together at defect site 154.

However, the above equation holds true even for general

leakage due to charge tunneling through the thin oxide --

that charge still has to travel along the two plates 148,

20   150 and will see the same resistance.

Supposing that a resistor of 35 ohms is included in the VDD - capactitor - resistor -ground layout to limit the leakage in the event of a defect. That 35 ohm resistor is there whether or not there is a leakage problem, and it will

5   serve as a bandwidth limiting resistance. In an exemplary embodiment of the invention, any leakage current will see roughly 35 ohms. But in normal operation only half that resistance exists. An added bonus is that without the gating device 102 or an actual added resistor 116 the layout

10   realizes a higher capacitance density.

Referring to Figures 8 and 9, a schematic representation of the invention includes polysilicon and diffusion plates 150, 148, respectively, or visa versa, V1 and V2 146a are contacts to a first supply and V3 and V4

15   144a are contacts to a second supply, as are also contacts V3' and V4'. D 154 is a defect, a short between the first plate 150 and second plate 148.

Figure 9 illustrates a model of the resultant capacitor as a distributed RC chain, showing defect D 154 in the

20   schematic. If D 154 exists, there is a resistance between the two supplies that is:

(2)   (Rv1 || Rv2) + R1 + R2 + R3 + R4A + (Rv3 || Rv4)

where || means "in parallel with".

Letting all R's be R and ignoring the small contact resistance, the result of equation (2) is 4*R. In terms of
5   frequency response (now assuming no defect 145) at infinite frequency, all the capacitors 156 become shorts. The series resistance is:

(3)   (Rv1 || Rv2) + (R1 || R1A) + (R2 || R2A) + (R3 || R3A)
      + (R4 || R4A) + (Rv3 || Rv4)

10   Again letting all the R's be R and ignoring the small contact resistors, the series resistance is simply 4*R/2 (in the example), that is 2*R. The leakage limiting resistance is 4*R while the bandwidth limiting resistance is only 2*R while a design using a separate series resistor would show
15   the same leakage and bandwidth limiting resistance.

Referring to Figure 10, in a typical package, diffusion layer 150 and polysilicon layer 148 provide a capacitor across the gate oxide insulation layer between ground and voltage. Defect 154 occurs in the gate oxide layer, in

5   effect shorting the ground and voltage plates.

Referring to Figure 11, typically a large plurality of voltage ties 158, 162 tie Vdd layer 150 to voltage, and a large plurality of ground ties 160, 164 tied the polysilicon layer 148 to ground.

10   Referring to Figure 12, the present invention achieves an improved package by, in effect, removing ties 158 and 160, leaving a much smaller and strategically positioned number of voltage contacts, or ties, 162 and ground ties 164. (One each is shown, but there will be as many as a

15   selected site allows). Thus, sites for voltage ties 162 and ground ties 164 are selected so as to maximize resistance paths R11 and R21 through any possible failure site 154, forcing current through defect 154 to pass from Vdd 162 to

Gnd 164 through diffusion resistance R11 and R21. The resulting series resistance is R11 + RS + R21.

As illustrated in Figures 13 and 14, the current flow from defect 154 to ground contacts 164 moves across the surface of the polysilicon layer 148, current 172, 174 flows to defect 154 from contacts 162a, 162, respectively in diffusion layer 150.

Referring to Figure 15, in accordance with the present invention, sites 164 and 162, or sites 164 and sites 162, 162a, are selected so as to maximize the distance K, thereby maximizing the sum of paths 170 + 172/174 to assure the maximum possible sheet resistance R11 + R21 through any defect site 154. The number of contacts at sites 164 and 162 and/or 162a is selected to be the maximum allowed a contact site. The site available for contacts 164 is provided by the extension of polysilicon plate beyond the polysilicon/diffusion overlap. The space available for contacts 162 site is the extension of the diffusion plate beyond the polysilicon/diffusion overlay which is separated from site 164 by at least distance K. This number of contacts 162, 164 is technology dependent, but selected such that the total contact resistance R is much less (by about

1/10) than combined sheet resistance of diffusion and polysilicon layers across distance K.

In the above described embodiment of the invention, the VDD bus is tied to the diffusion (bottom plate) and the GND bus is tied to the polysilicon (top plate). This is the preferred embodiment when using a large PFET to create the capacitor. In current technology, the pcap design gives a higher density layout (i.e. capacitance/layout area) than an NFET design. However, in an alternative embodiment, the present invention also applies to an NFET design where the polysilicon is tied to the VDD and diffusion is tied to GND.

Referring to Figure 16, a method for determining the number and position of contacts is to calculate in step 182 the minimum sheet resistance value R determined in step 180 that is needed to limit defect current to an amount which allows IDDQ testing, and in step 184 use that R value to determine the distance K between contacts 164, 162. IDDQ is basically the DC current of the circuit while nothing is switching. Assuming that 1/2 of R is in the polysilicon layer and 1/2 in the diffusion layer, for a give sheet resistance, in step 186, the number of contacts N needed to provide a sufficiently low contact resistance to assure that

sheet resistance dominates is determined, and in step 188

contact sites are designed of sufficient area and distance K

to provide for placement of N contacts. Defect current and

frequency specifications depend on the technology and the

5   application for the circuit. In general, such

specifications are set so as to allow IDDQ testing and

achieve stable busses by suppressing, substantially limiting

or eliminating noise on the Vdd and ground busses.

Alternative Embodiments

10   It will be appreciated that, although specific

embodiments of the invention have been described herein for

purposes of illustration, various modifications may be made

without departing from the spirit and scope of the

invention. Referring to Figure 17, in particular, it is

15   within the scope of the invention to provide a computer

program product or program element, or a program storage or

memory device 200 such as a solid or fluid transmission

medium, magnetic or optical wire, tape or disc, or the like,

for storing signals readable by a machine as is illustrated

20   by line 202, for controlling the operation of a computer

204, such as a host system or storage controller, according

to the method of the invention and/or to structure its components in accordance with the system of the invention.

Further, each step of the method may be executed on any general purpose computer, such as IBM Systems designated as zSeries, iSeries, xSeries, and pSeries, or the like and pursuant to one or more, or a part of one or more, program elements, modules or objects generated from any programming language, such as C++, Java, Pl/1, Fortran or the like. And still further, each said step, or a file or object or the like implementing each said step, may be executed by special purpose hardware or a circuit module designed for that purpose.

Accordingly, the scope of protection of this invention is limited only by the following claims and their equivalents.